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First Named Inventor (or identifier)	Chen-Chih HUANG
Total Pages	33

This submits a new application under 37 CFR 1.53(b).

Entitled: MULTI-PHASE-LOCKED LOOP FOR DATA RECOVERY

☒ 1. Submitted herewith are the following:

_16_ pages of specification, including an Abstract,
_8_ sheet(s) of drawings, and
_4_ claim(s).

☒ 2. Submitted herewith is an Oath/Declaration signed by each inventor.

☒ 3. Submitted herewith are the following:
- ☐ __ signed Independent Inventor Small Entity Statement(s),
- ☒ 1 signed Small Business Small Entity Statement(s),
- ☐ __ signed Non-Profit Small Entity Statement(s).
- ☐ __ signed Non-Inventor Small Entity Statement(s),

☐ 4. A preliminary amendment is enclosed.

☐ 5. Submitted herewith is an Information Disclosure Statement, ___ pages of Form PTO-1449, and one copy of each document listed thereon.

☒ 6. An assignment of the invention to REALTEK Semiconductor Corp.

☐ 7. A certified copy of application no. _____ in _____.

☒ 8. The Commissioner is authorized to credit any over payment and charge any deficiency in any fees required under 37 CFR 1.16, 1.17 and/or 1.18, to Deposit Account No. 02-0200.

☒ 9. A check in the amount of $ 420.00 is submitted herewith.

☐ 10. Other:_____

THE FILING FEE IS CALCULATED AS FOLLOWS:				Basic Fee:	$760.00
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June 14, 1999	Eugene Mar		25,893

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VERIFIED STATEMENT (DECLARATION) BY A SMALL BUSINESS CLAIMING SMALL ENTITY STATUS UNDER *37 CFR 1.9(F) AND 1.27(b)*

Applicant or Patentee: Chen-chih HUANG | Docket #:

Serial or Patent Number: | Group Art Unit:

Filed or Issued: | Examiner:

Title: MULTI-PHASE-LOCKED LOOP FOR DATA RECOVERY

I hereby declare that I am
- ☒ the owner of the small business concern identified below:
- ☐ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Concern:REALTEK Semiconductor Corp.
Address. No. 2, Industry E.Road IX, Science-Based Industrial Park, Hsinchu, 300 Taiwan, R.O.C.

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the matter described in:
- ☒ The specification filed herewith, with the title as listed above.
- ☐ The patent application identified above.
- ☐ The PCT international patent application identified above.
- ☐ The patent number identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under *37 CFR 1.9(c)* if that person made the invention, or by any concern who would not qualify as a small business concern under *37 CFR 1.9(e)*. Each person or organization having any rights in the invention is listed below:
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FULL NAME:	☐ Individual
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☐ See attached sheet for additional person(s) concern(s) or organization(s).

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate *(37 CFR 1.28(b))*.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under *section 1001 of Title 18 of the United States Code*, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which the verified statement is directed.

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MULTI-PHASE-LOCKED LOOP FOR DATA RECOVERY

FIELD OF THE INVENTION

The present invention relates generally to a phase-locked loop for data recovery, and more particularly, to a multi-phase-locked loop that utilizes a multi-phase clock signal generated by a multi-phase voltage controlled oscillator (VCO) to detect received data.

BACKGROUND OF THE INVENTION

Due to the development of the network transmission technology as well as the demands in the installed base of computer networks, the network data transmission rate in hardware environment has been increased. Therefore, it becomes more and more important to recover data (clock signals) correctly.

At present, while data (clock) recovery is to be performed, a phase-locked loop is often utilized. During the data recovery process, usually the received data could be correctly recovered (read) by using a phase detector to synchronize the received data and recover the clock. In other words, the phase detector plays a very important role whether the data could be correctly recovered by a phase-locked loop.

FIG. 1 illustrates a prior art phase-locked loop for data recovery comprising a phase detector 11, a charge pump 12, a loop filter 13, and a voltage controlled oscillator 14. The phase detector 11 is used to receive a data (clock) signal from outside as well as a feedback

clock signal CK_{vco} from the voltage controlled oscillator 14. The phase detector 11 compares the two signals, in accordance with their phase difference θ_e ($\theta_e=\theta_{data}-\theta_{clock}$), a control signal *up* or *dn* will be output to control the charge pump 12. As shown in FIG. 2(a), when the transition edge of the data (clock) signal *data* leads the falling edge of the feedback clock signal CK_{vco}, the phase detector outputs an *up* signal. On the other hand, as shown in FIG. 2(b), when the transition edge of the data (clock) signal *data* lags behind the falling edge of the feedback clock signal CK_{vco}, the phase detector 11 outputs a *dn* signal. The charge pump 12 is controlled by the *up* and *dn* control signals output from the phase detector 11 to perform charge/discharge operations, and generates a voltage signal *Vd*. The loop filter 13 receives the voltage signal *Vd* and generates an appropriate voltage *Vc* for controlling the voltage controlled oscillator 14. The voltage controlled oscillator 14 receives the voltage *Vc* and generates a clock signal CK_{vco} to be input to the phase detector 11.

As shown in FIG. 3, the phase detector 11 of the phase locked loop 1 is constituted by four flip-flops 111, 112, 113,114, and two OR gates 115, 116. The flip-flops 111 and 112 receive the complement of data from outside (denoted by $\overline{data}$) and the data itself (denoted by *data*), respectively. The clock signal CK_{vco} from the voltage controlled oscillator 14 is applied to the inversion reset terminals (rb) of the flip-flops 111 and 112 such that two control signals *up1* and *up2* are generated, respectively. The flip-flops 113 and 114 receive the

complement of data from outside (denoted by $\overline{data}$) and the data itself (denoted by *data*), respectively. The complement of the clock signal CK_{vco} (denoted by $\overline{CK_{vco}}$) from the voltage controlled oscillator 14 is applied to the inversion reset terminals (rb) of the flip-flops 113 and 114 such that two control signals *dn1* and *dn2* are generated, respectively. According to the two signals up_1 and up_2, the OR gate 115 generates a control signal *up* for controlling the charge pump 12 (refer to FIG. 2 (a)). Similarly, the OR gate 116 generates a control signal *dn* for controlling the charge pump 12 according to the two signals dn_1 and dn_2 (refer to FIG. 2 (b)).

Referring to FIG. 1, the voltage *Vd* is substantially controlled by the signals (*up, dn*). In other words, the variation of the control voltage *Vd* is related to the phase error θ_e. FIG. 4 illustrates the relation between the variation of *Vd* and the phase error θ_e. As shown in FIG. 4, when the data signal *data* has a phase lagging behind the clock signal CK_{vco}, the smaller the phase error θ_e is, the more the voltage *Vd* varies. Therefore, phase error θ_e is theoretically supposed to approximate to zero and closely moves around the origin when the phase-locked loop is going to enter a phase-locked state. However, due to the above phenomenon, when the data signal *data* of the phase-locked loop has a phase lagging behind the clock signal CK_{vco}, an obvious variation of *Vd* will be generated, which leads to clock jitter. And, the tolerance for data random jitter becomes worse. In other words, it is difficult to reduce the clock jitter for conventional phase-locked loops, large data random

jitter is thus unaccepted.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a multi-phase-locked loop without dead zone, which can reduce clock jitter and provide higher tolerance for data random jitter.

Another object of the present invention is to provide a multi-phase-locked loop without static phase error.

The present invention is characterized by a multi-phase-locked loop which can generate a plurality of multi-phase clock signals by a multi-phase voltage controlled oscillater to detect the transition edge of the data signal *data*. Accordingly, multiple sets of control signals (up_k/dn_k) are generated. Therefore, phase error θ_e and voltage *Vd* of the multi-phase-locked loop can be adjusted to be nearly linear according to the output control signals. This prevents the multi-phase-locked loop from having dead zone. Furthermore, the clock jitter can be reduced and provide greater tolerance for data random jitter.

To achieve the aforementioned object, a multi-phase-locked loop for data recovery in accordance with the invention includes a phase detector, a charge pump, a loop filter and a voltage controlled oscillator (VCO).

The phase detector is constituted by N phase detection units (U_1, U_2, ..., U_N, N is even, $N \geqq 4$). The phase detection units are connected in cascade configuration, and each of the phase detection unit contains a data signal input terminal for receiving the data signal from

outside; a clock signal input terminal for receiving the multi-phase clock signals (CK_1, CK_2,..., CK_N) from outside; a delay signal input terminal for receiving the delay signal output from another phase detection unit; a delay signal output terminal for outputting the delay signal; and a charge/discharge control signal output terminal for outputting charge/discharge control signals. Each phase detection unit generates a delay signal (D_1, D_2,..., D_N) according to the input data signal and the complement of the multi-phase clock signal.

The delay signal (D_{j+1}) generated by the $(j+1)_{th}$ phase detection unit is applied to the j_{th} phase detection unit via the j_{th} delay signal input terminal. The delay signal (D_1) generated by the first phase detection unit (U_1) is applied to the N_{th} phase detection unit (U_N) via the N_{th} delay signal input terminal. In addition, the j_{th} phase detection unit (U_j, $1 \leqq j \leqq N$, j is an integer) generates control signals (dn_1, dn_2,..., $dn_{N/2}$, $up_{N/2}$,..., up_2) for the charge/discharge operations according to the delay signal (D_j) from the j_{th} phase detection unit, the delay signal (D_{j+1}) from the $(j+1)_{th}$ phase detection unit, and the multi-phase clock signal (CK_j) which is applied to the j_{th} phase detection unit. However, the N_{th} phase detection unit (U_N) generates a charge control signal (up_1) according to the delay signal (D_N) from the N_{th} phase detection unit, the delay signal (D_1) from the first phase detection unit, and the multi-phase clock signal (CK_N) which is applied to the N_{th} phase detection unit.

The charge pump is constituted by N/2 charge and discharge units (CP_1, CP_2,..., $CP_{N/2}$), wherein the k_{th} (1

$\leqq k \leqq N/2$) charge and discharge unit (CP_k) receives the k_{th} charge/discharge control signal (up_k/dn_k) from the above mentioned phase detector and generates a charge/discharge current Ich_k, which equals to ($w_k \times up_k - w_k \times dn_k$) Iss, wherein w_k is a weighting value; Iss is a fixed current value; and $w_1 < w_2 < \ldots < w_{N/2}$. The total charge/discharge current (Ich) output from the charge pump equals to $Ich_1 + Ich_2 + \ldots Ich_k + \ldots + Ich_{N/2}$.

The VCO described above is a multi-phase VCO, it outputs N multi-phase clock signals (CK_1, $CK_2 \ldots$, CK_N). These signals are applied to the phase detectors described above, respectively.

Under the circumstance described above, the phase difference between CK_{j+1} and CK_j is $2\pi/N$.

The multi-phase clock signal (CK_{j+1}) which is applied to the $(j+1)_{th}$ phase detection unit (U_{j+1}) and the multi-phase clock signal (CK_j) which is applied to the j_{th} phase detection unit (U_j). In accordance with the invention, the relation between the phase error θ_e and the voltage *Vd* of the phase-locked loop can be adjusted to be nearly linear by employing these control signals. Therefore, a phase-locked loop without dead zone can be derived, which can reduce clock jitter and enhance the tolerance for data random jitter.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and the features and effects of the present invention can be best understood by referring to the following detailed descriptions of the preferred embodiment and the accompanying drawings,

in which:

FIG. 1 is a block diagram showing a prior art phase-locked loop for data recovery;

FIG. 2 (a) is a clock diagram showing the control signal (*up*) generated by a prior art phase detector when the transition edge of the data signal *data* leads the falling edge of the clock signal CK_{vco};

FIG. 2 (b) is a clock diagram showing the control signal (*dn*) generated by a prior art phase detector when the transition edge of the data signal *data* lags behind the falling edge of the clock signal CK_{vco};

FIG. 3 depicts a circuit of a prior art phase detector;

FIG. 4 depicts the relation between the phase error θ_e and voltage *Vd* by using a prior art phase detector;

FIG. 5 is a block diagram showing a multi-phase-locked loop in accordance with the present invention;

FIG. 6 is a block diagram showing a phase detector in accordance with the present invention;

FIG. 7 is a detailed circuit showing a phase detector in accordance with the present invention;

FIG. 8 is a detailed circuit showing a charge pump in accordance with the present invention;

FIG. 9 is a state diagram showing the signals of data signal *data* employed in the multi-phase-locked loop, the multi-phase clock signals (CK_1, CK_2, ..., CK_{10}), and the charge/discharge control signals (up_k/dn_k) used in the present invention; and

FIG. 10 depicts the relation between the phase error θ_e and voltage *Vd* in the multi-phase-locked loop in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before describing the preferred embodiment in accordance with the invention, it should be made clear that the loop filter in the multi-phase-locked loop of the invention are similar to that of the prior art and will not be explained here.

Firstly, referring to FIG. 5, the multi-phase-locked loop for data recovery in accordance with the invention includes: a phase detector 21, a charge pump22, a loop filter 23, and a multi-phase VCO 24.

As illustrated in FIG. 6, the phase detector 21 is constituted by N phase detection units (U_1, U_2,..., U_N), wherein N is even and $N \geqq 4$. The phase detection units (U_1, U_2,..., U_N) are connected in cascade configuration, and each phase detection unit contains: a data signal input terminal 61 for receiving a data signal from outside; a clock signal input terminal 62 for receiving multi-phase clock signals (CK_1, CK_2,..., CK_N) from outside; a delay signal input terminal 63 for receiving the output delay signal from another phase detection unit; a delay signal output terminal 64 for outputting a elay signal; and a charge/discharge control signal output terminal 65 for outputting charge/discharge control signal.

Each phase detection unit (U_1,U_2...U_N) generates a delay signal (D_1, D_2, ..., D_N) according to the data signal *data* applied to the phase detection unit, and the complement of the multi-phase clock signals (CK_1, CK_2,..., CK_N). Moreover, the delay signal (D_{j+1}) generated by the $(j+1)_{th}$ phase detection unit(U_{j+1}) is applied to the j_{th}

phase detection unit (U_j) via the delay signal input terminal 63 in the j_{th} phase detection unit(U_j). And the delay signal (D_1) generated by the first phase detection unit(U_1) is applied to the N_{th} phase detection unit (U_N) via the delay signal input terminal 63 in the N_{th} phase detection unit (U_N).

The j_{th} phase detection unit (U_j, $1 \leqq j < N$, j is a positive integer) generates charge/discharge control signals (dn_1, $dn_2, \ldots, dn_{N/2}$, $up_{N/2}, \ldots, up_2$) according to the delay signal (D_j) from the j_{th} phase detection unit(U_j), the delay signal (D_{j+1}) from the $(j+1)_{th}$ phase detection unit(U_{j+1}), and the multi-phase clock signal(CK_j) which is applied to the j_{th} phase detection unit(U_j). The N_{th} phase detection unit generates a charge control signal (up_1) according to the delay signal (D_n) from the N_{th} phase detection unit(U_N), the delay signal (D_1) from the first phase detection unit(U_1), and the multi-phase clock signal(CK_N) which is applied to the N_{th} phase detection unit(U_N).

As described above, the multi-phase clock signal (CK_{j+1}) is applied to the $(j+1)_{th}$ phase detection unit (U_{j+1}) and the multi-phase clock signal (CK_j) is applied to the j_{th} phase detection unit (U_j). The phase difference between the two signals is $2\pi/N$. Moreover, as described above, the plurality of multi-phase clock signals (CK_1, $CK_2, \ldots,$ CK_N) are generated by the VCO 24.

Furthermore, FIG. 7 is utilized to illustrate the detailed circuit of phase detector 21 in accordance with the invention. As shown in FIG. 7, each phase detection unit (U_1, $U_2, \ldots, U_N$) of the phase detector 21 in accordance with the invention includes: an inverter 211, a first

flip-flop 212, an exclusive OR gate 213, and a second flip-flop 214. The inverter 211 inverts the multi-phase clock signals (CK_1, CK_2, ..., CK_N) before these signals are applied to each first flip-flop 212, respectively. Each of the first flip-flops 212 generates a delay signal D_i ($1 \leqq i \leqq N$) according to the above mentioned data signal *data*, and the multi-phase clock signal which has been inverted by the inverter 2. The delay signal (D_j) from the first flip-flop 212 and the delay signal (D_{j+1}) from the first flip-flop 212 in next phase detection unit, are both applied to the exclusive OR gate 213. The second flip-flop 214 generates charge/discharge control signals (dn_1, dn_2, ..., $dn_{N/2}$, $up_{N/2}$, ..., up_2) according to the above mentioned multi-phase clock signal and the signal output from the exclusive OR gate.

It should be mentioned that the charge control signal (up_1) is generated by the second flip-flop 214 of the N_{th} phase detection unit (U_N), which is based on the above described multi-phase clock signal (CK_N) and the output signal from its exclusive OR gate 213. The input signals of the exclusive OR gate 213 of the N_{th} phase detection unit (U_N) are the delay signal (D_1) from the first phase detection unit (U_1) and the delay signal (D_N) from itself. In addition, the first flip-flop and the second flip-flop are both D flip-flops in this embodiment.

As shown in FIG. 8, the charge pump 22 is constituted by N/2 charge and discharge units (CP_1, CP_2, ..., $CP_{N/2}$). The k_{th} charge and discharge unit CP_k ($1 \leqq k \leqq N/2$) receives the k_{th} charge/discharge control signal ($up_k \cdot dn_k$) output from the phase detector 21 and generates a

charge/discharge current Ich_k according to the received signal. The charge/discharge current Ich_k is determined by: $(w_k \times up_k - w_k \times dn_k)\,Iss$, wherein w_k is a weighting value, Iss is a fixed current value, and $w_1 < w_2 < \ldots < w_{N/2}$. Therefore, the total charge/discharge current (Ich) output from charge pump 22 is:

$$Ich = Ich_1 + Ich_2 + \ldots Ich_k + \ldots + Ich_{N/2}$$

In other words, the total charge/discharge current (Ich) is:

$$Ich = \{[w_1 \times up_1 + w_2 \times up_2 + \ldots + w_{N/2} \times up_{N/2}] - [w_1 \times dn_1 + w_2 \times dn_2 + \ldots + w_{N/2} \times dn_{N/2}]\}Iss$$

A exemplified configuration of the multi-phase-locked loop is depicted below to further explain the method of using a couple of multi-phase clock signals.

【EXEMPLIFIED CONFIGURATION】

Firstly it should be mentioned here, the preferred embodiment recited below includes ten phase detection units (U_1, U_2, ..., U_{10}) in the phase detector 21.

Secondly, referring to FIG. 7, when the data signal *data* and the multi-phase clock signal (CK_1, CK_2, ..., CK_{10}) shown in FIG. 9 are applied to each phase detection unit (U_1, U_2, ..., U_{10}), the first flip-flop 212 of the first phase detection unit (U_1) outputs a delay signal (D_1); the first flip-flop 212 of the second phase detection unit (U_2) outputs a delay signal (D_2);...etc.

As described above, the delay signal (D_1) generated by the first phase detection unit (U_1) as well as the delay signal (D_2) generated by the second phase detection unit (U_2) cooperatively generate an output signal ($D_1 \oplus D2$) via

the exclusive OR gate 213 in the first phase detection unit (U_1). Similarly, the delay signal (D_2) generated by the second phase detection unit (U_2) as well as the delay signal (D_3) generated by the third phase detection unit (U_3) cooperatively generate an output signal ($D2 \oplus D3$) via the exclusive OR gate 213 in the second phase detection unit (U_2). However, the delay signal (D_{10}) generated by the tenth phase detection unit (U_{10}) as well as the delay signal (D_1) generated by the first phase detection unit (U_1) cooperatively generate an output signal ($D_{10} \oplus D_1$) via the exclusive OR gate 213 in the tenth phase detection unit (U_{10}).

As described in the preceding paragraph, the second flip-flop 214 of the first phase detection unit (U_1) generates a discharge control signal (dn_1) according to the multi-phase clock signal (CK_1) and the output signal ($D_1 \oplus D_2$) from the exclusive OR gate 213. Similarly, the second flip-flop 214 of the second phase detection unit (U_2) generates a discharge control signal (dn_2) according to the multi-phase clock signal (CK_2) and the output signal ($D_2 \oplus D_3$) from the exclusive OR gate 213. Similarly as above, the third to fifth phase detection units ($U_3 \sim U_5$) generates a discharge control signal ($dn_3 \sim dn_5$), respectively. Furthermore, the sixth to ninth phase detection units ($U_6 \sim U_9$) generates a charge control signal ($up_5 \sim up_2$). The second flip-flop 214 of the tenth phase detection unit (U_{10}) generates a charge control signal (up_1) according to the multi-phase clock signal (CK_{10}) and the output signal from the exclusive OR gate 213. It should be mentioned here, due to the phase difference

between two consecutive multi-phase clock signals of (CK_1, CK_2, ..., CK_{10}) being $2\pi/10$, the phase detection unit (U_1, U_2, ..., U_{10}) of the phase detector 21 respectively generate five discharge control signals (dn_1、dn_2、dn_3、dn_4、dn_5) and five charge control signals (up_1、up_2、up_3、up_4、up_5) in this preferred embodiment.

Referring to FIG. 8, the phase detector 21 in this preferred embodiment includes ten phase detection units (U_1, U_2, ..., U_{10}), the charge pump 22 contains five charge and discharge units (CP_1, CP_2, ..., CP_5). At this time, the charge/discharge control signals (up_1/dn_1、up_2/dn_2、up_3/dn_3、up_4/dn_4、up_5/dn_5) output from the phase detector 21 are respectively applied to the charge and discharge units (CP_1, CP_2, ..., CP_5). If $Ich(t)$ represents the total charge/discharge current of charge pump 22 at time t, Iss represents a fixed current value, and w_1~w_5 represent the weighting value of each charge and discharge unit, wherein $w_1<w_2<w_3<w_4<w_5$, then,

$$I_{ch}(t)=$$

$$\{[w_1\times up_1(t)+w_2\times up_2(t)+w_3\times up_3(t)+w_4\times up_4(t)+w_5\times up_5(t)]-$$

$$[w_1\times dn_1(t)+w_2\times dn_2(t)+w_3\times dn_3(t)+w_4\times dn_4(t)+w_5\times dn_5(t)]\}Iss$$

Consequently, it is obvious that the total charge/discharge current Ich output from the charge pump 22 displays a nearly linear variation in the multi-phase-locked loop of this preferred embodiment. Therefore, the phase error θ_e and the voltage Vd in the multi-phase-locked loop in accordance with the invention can be adjusted to be nearly linear (as shown in FIG. 10)

according to those control signals.

To sum up, there are some advantages in the multi-phase-locked loop in accordance with the invention, which are listed as follows:

1. From FIG. 10, it can be understood that there is no dead zone in the multi-phase-locked loop in accordance with the invention because all the *up/dn* are kept as a fixed time period. Therefore, enough long signals (*up* or *dn*) can be generated even the phase error θ_e is very small.

2. Due to the linear relation between *Vd* and θ_e, a sudden voltage variation can be avoided. The condition illustrated in FIG. 4 can thus be prevented, and smaller recovering clock jitter can be acquired as well.

3. Larger tolerance for data random jitter can also be derived because lower recovering clock jitter can be acquired by the phase detector in accordance with the invention.

4. When the conventional phase detector 11 as illustrated in FIG. 1 is used to recover the data, another flip-flop needs to be incorporated to read the data in a steady locked phase. Therefore, the problems such as device coupling, parasitic capacitance and delay effects cannot be avoided, which is called static phase error. On the other hand, it is unnecessary to add another flip-flop to read the data in a steady locked phase by using CK_6 to recover (read) data directly in the phase detector according to the invention to get the best recovered data (D_6, not shown in the figure).

The exemplified configuration and the preferred embodiment described in the description are only

illustrative and are not to be construed as limiting the invention. Various modifications and applications can be made without departing from the true spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A multi-phase-locked loop for data recovery comprising a phase detector, a charge pump, a loop filter and a voltage controlled oscillator, wherein:

said phase detector is constituted by N phase detection units (U_1, U_2, ..., U_N, N is even, $N \geq 4$); said N phase detection units are connected in cascade configuration, and each phase detection unit contains a data signal input terminal for receiving a data signal from outside; a clock signal input terminal for receiving the multi-phase clock signals (CK_1, CK_2, ..., CK_N) from outside; a delay signal input terminal for receiving a delay signal output from another phase detection unit; a delay signal output terminal for outputting a delay signal; and a charge/discharge control signal output terminal for outputting control signals for charge/discharge operations; each of said N phase detection units generates a delay signal (D_1, D_2, ..., D_N) according to an input data signal and the complement of a multi-phase clock signal; the delay signal (D_{j+1}) generated by the $(j+1)_{th}$ phase detection unit is input into the j_{th} phase detection unit via the j_{th} delay signal input terminal; the delay signal (D_1) generated by the first phase detection unit is input into the N_{th} phase detection unit via the N_{th} delay signal input terminal; the j_{th} phase detection unit (U_j, $1 \leq j < N$, j is a positive integer) generates control signals (dn_1, dn_2, ..., $dn_{N/2}$, $up_{N/2}$, ..., up_2) for charge/discharge operations according to the delay signal (D_j) from the j_{th} phase detection unit, the

delay signal (D_{j+1}) from the $(j+1)_{th}$ phase detection unit, and the multi-phase clock signal (CK_j) which is applied to the j_{th} phase detection unit; the N_{th} phase detection unit generates a charge control signal (up_1) according to the delay signal (D_n) from the N_{th} phase detection unit, the delay signal (D_1) from the first phase detection unit, and the multi-phase clock signal (CK_N) which is applied to the N_{th} phase detection unit;

said charge pump being constituted by N/2 charge and discharge units (CP_1, CP_2,..., $CP_{N/2}$), wherein the k_{th} (CP_k, $1 \le k \le N/2$) charge and discharge unit (CP_k) is employed to receive the k_{th} charge/discharge control signal set (up_k/dn_k) from said phase detector, and a current Ich_k is generated by the charge/discharge control signal set (up_k/dn_k); the charge/discharge current $Ich_k = (w_k \times up_k - w_k \times dn_k) Iss$, wherein w_k is a weighting value, Iss is a fixed current value, and $w_1 < w_2 < \ldots < w_{N/2}$; the total charge/discharge current (Ich) from said charge pump equals to $Ich_1 + Ich_2 + \ldots Ich_k + \ldots + Ich_{N/2}$; and said voltage controlled oscillator is a multi-phase voltage controlled oscillator, which outputs N multi-phase clock signals (CK_1, CK_2..., CK_N), which are applied to said phase detectors, respectively.

2.The multi-phase-locked loop for data recovery as described in claim 1, wherein the phase difference between the multi-phase clock signal (CK_{j+1}) input to the $(j+1)_{th}$ phase detection unit (U_{j+1}) and the multi-phase clock signal (CK_j) input to the j_{th} phase detection unit (U_j) equals to $2\pi/N$.

3.The multi-phase-locked loop for data recovery as

described in claim 1, wherein each of said N phase detection unit comprises: an inverter, a first flip-flop, an exclusive OR gate, and a second flip-flop;

said inverter inverting multi-phase clock signal which is to be input to each phase detection unit; the first flip-flop generating a delay signal according to the complementary multi-phase clock signal from said inverter and the data signal; the delay signal from said first flip-flop and the delay signal from the first flip-flop in another phase detection unit being input to the exclusive OR gate; the second flip-flop generating a charge/discharge control signal according to the multi-phase clock signal and the output signal from said exclusive OR gate.

4.The multi-phase-locked loop for data recovery as described in claim 2, wherein said first flip-flop and said second flip-flop are D flip-flops.

ABSTRACT OF THE DISCLOSURE

The present invention provides a multi-phase-locked loop without dead zone, which can reduce clock jitter and provide larger tolerance for data random jitter. It generates and output multiple sets of control signals (up_k/dn_k) via a multi-phase voltage controlled oscillator which generates a plurality of multi-phase clock signals for detecting the transition edge of data signal. Therefore, the phase error θ_e and the voltage *Vd* of the multi-phase-locked loop can be adjusted to be nearly linear according to the control signals. A multi-phase-locked loop without dead zone thus can be provided.

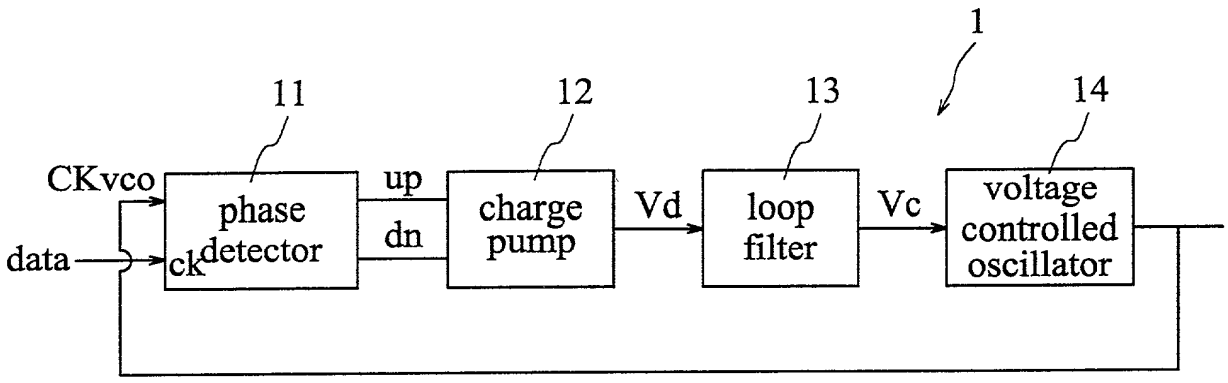

FIG. 1
(PRIOR ART)

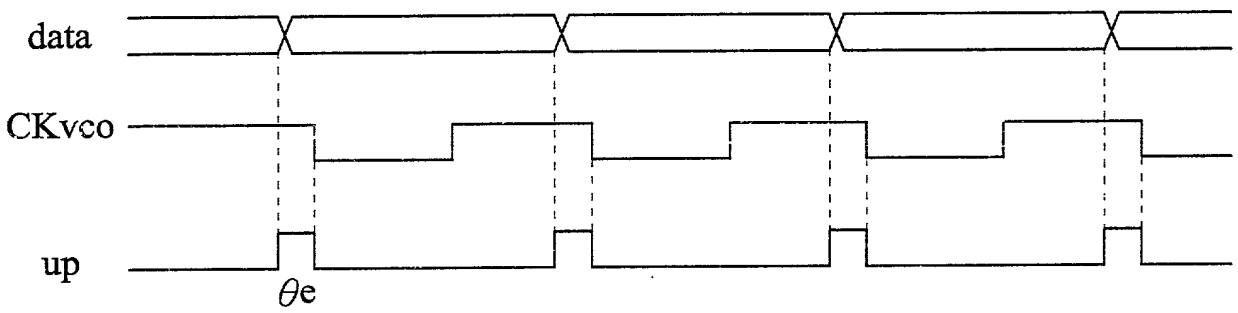

FIG. 2(a)

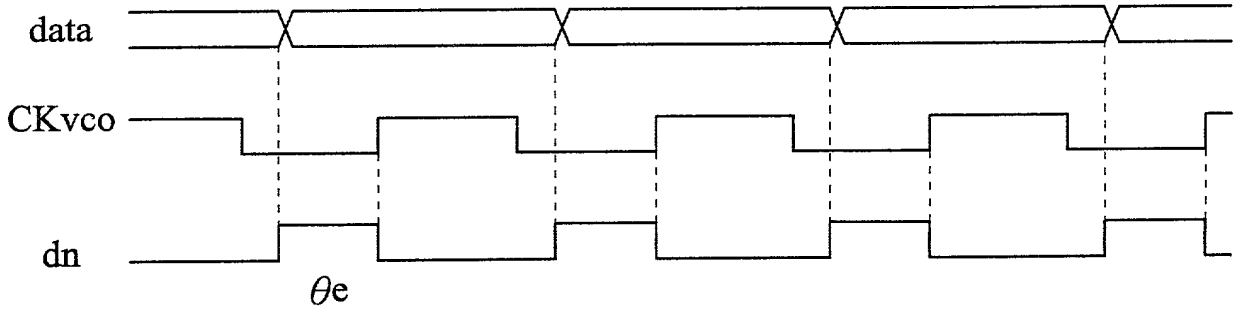

FIG. 2(b)

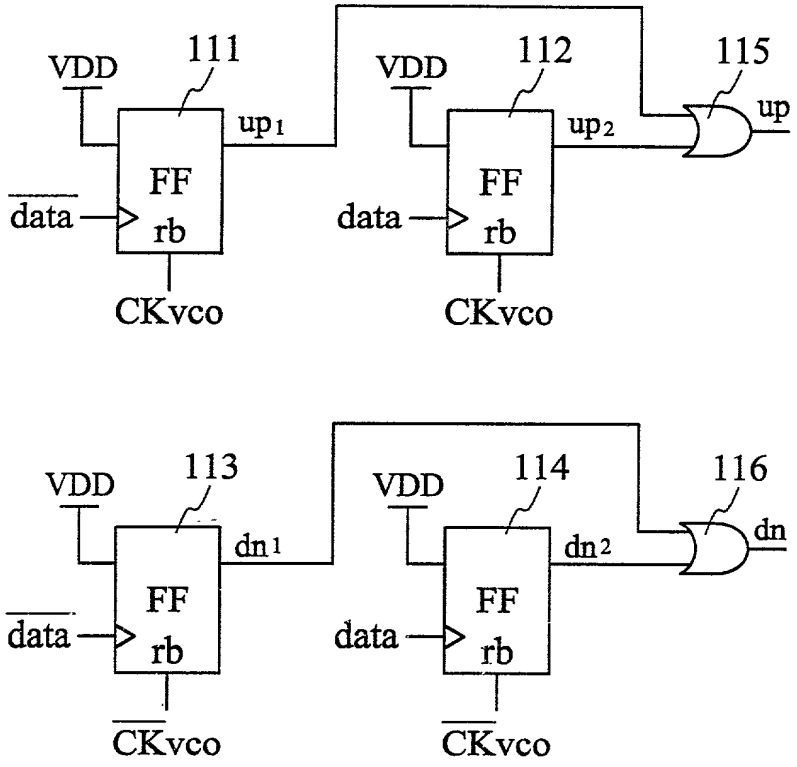
VDD
111
up1
FF
rb
data
CKvco
VDD
112
up2
FF
rb
data
CKvco
115
up
VDD
113
dn1
FF
rb
data
CKvco
VDD
114
dn2
FF
rb
data
CKvco
116
dn

FIG. 3

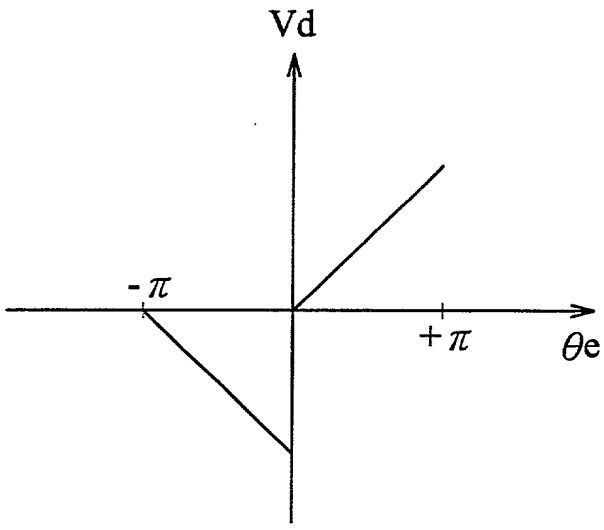
Vd
-π
+π
θe

FIG. 4

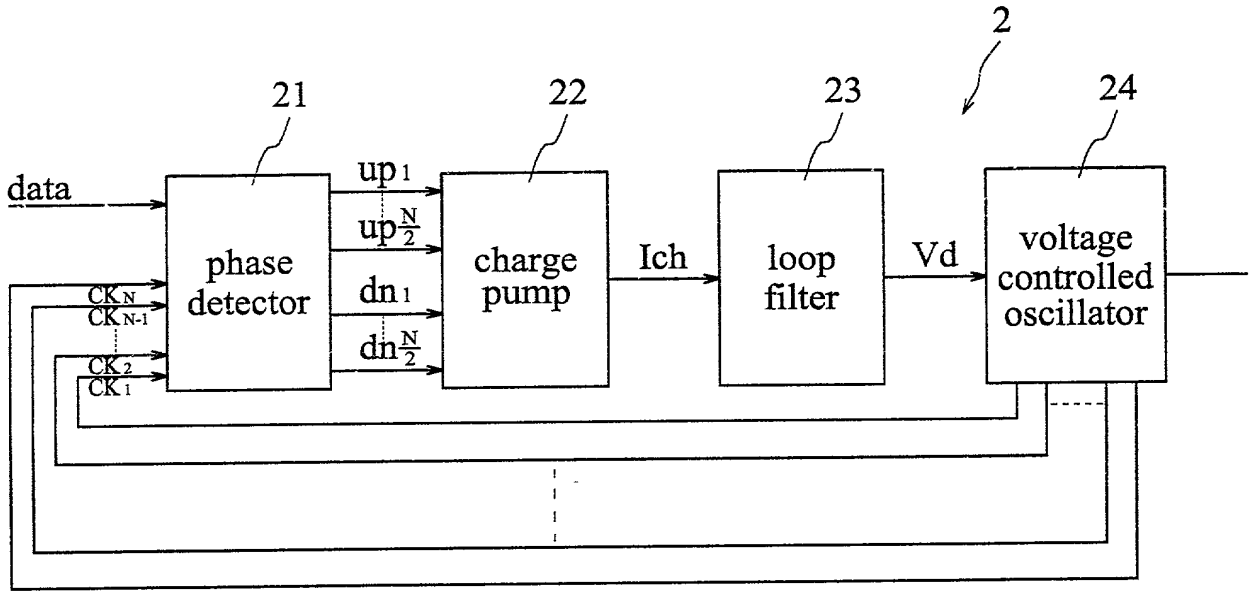

FIG. 5

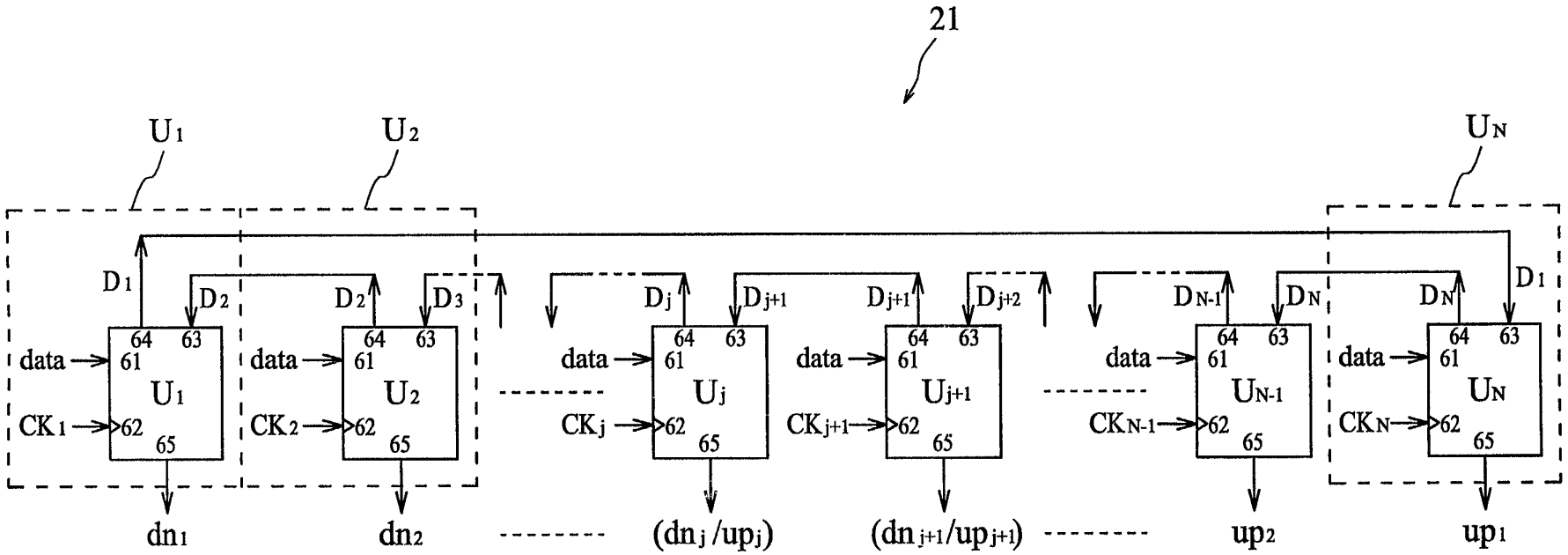

FIG. 6

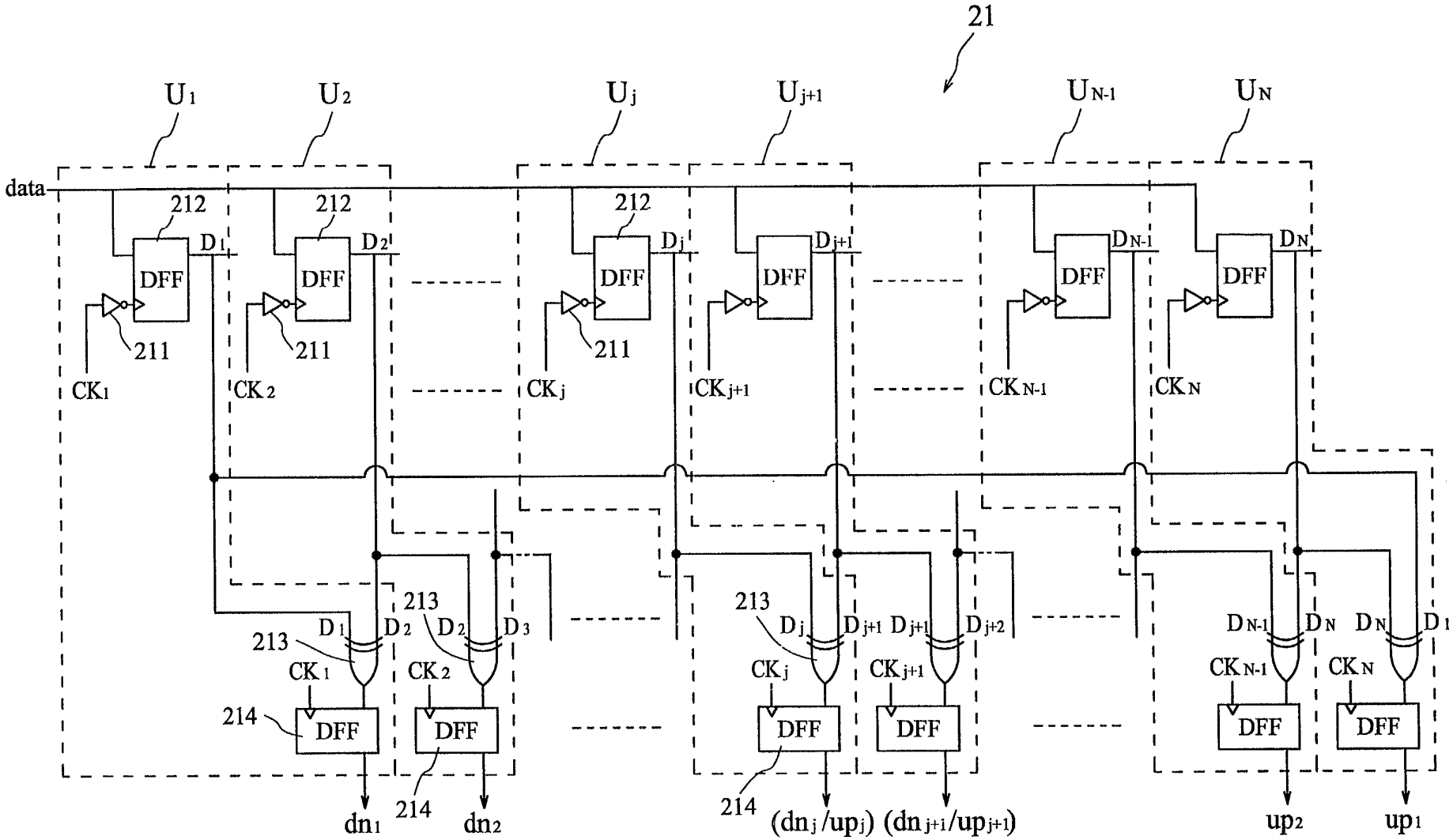

FIG. 7

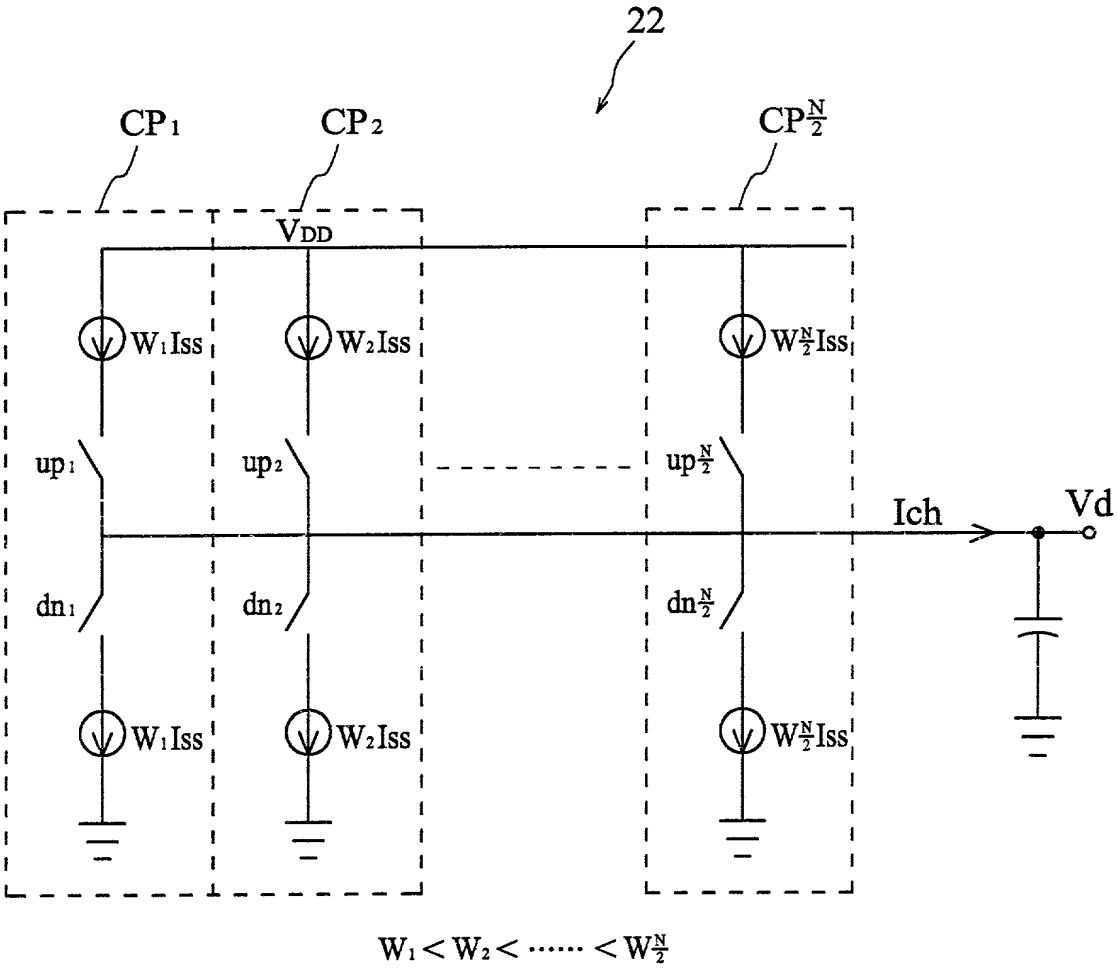
22
CP1
CP2
CP N/2
VDD
W1Iss
W2Iss
W N/2 Iss
up1
up2
up N/2
Ich
Vd
dn1
dn2
dn N/2
W1Iss
W2Iss
W N/2 Iss
W1 < W2 < ····· < W N/2

FIG. 8

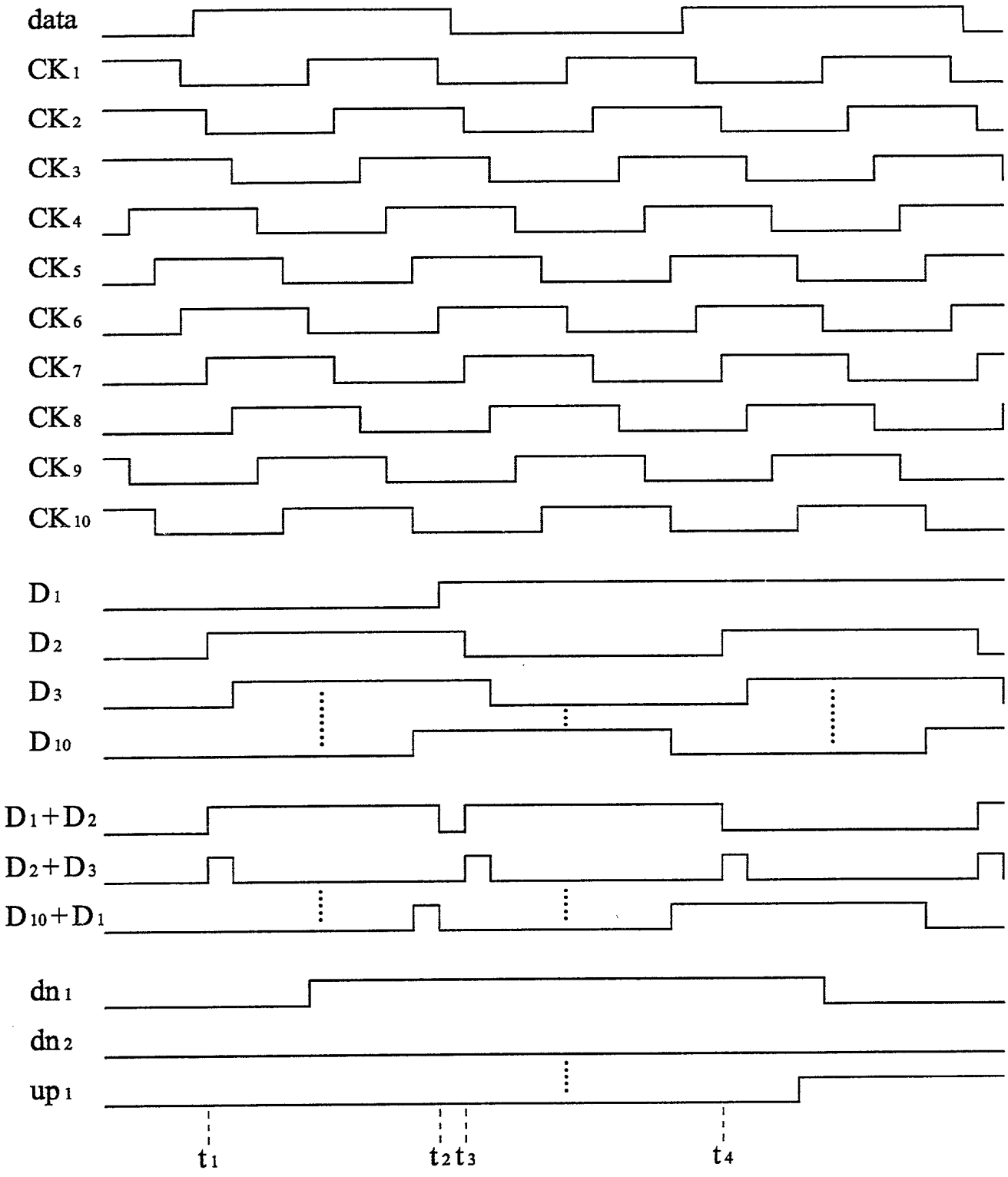
data
CK1
CK2
CK3
CK4
CK5
CK6
CK7
CK8
CK9
CK10
D1
D2
D3
D10
D1+D2
D2+D3
D10+D1
dn1
dn2
up1
t1
t2
t3
t4

FIG. 9

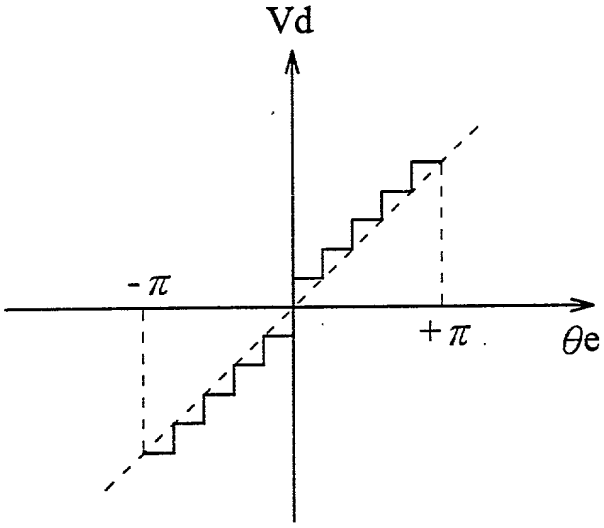

FIG. 10

DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:

MULTI-PHASE-LOCKED LOOP FOR DATA RECOVERY

the specification of which (check one):

☒ is attached hereto, or ☐ was filed on: as U.S. Application Number of PCT International Application Number:

and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations,* § *1.56.* I hereby claim foreign priority benefits under *Title 35, United States Code* § *119* of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	**Country**	**Day/Month/Year Filed**	**Yes**	**No**
Not yet assigned	Taiwan	21/5/1999		X

☐ Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE § 119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.	
Application Number	**Day/Month/Year Filed**

☐ Additional Provisional Application(s) Listed on Following Page(s)

☐ I hereby claim the benefit under *Title 35, United States Code,* § *120* of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of *Title 35, United States Code,* § *112,* I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations,* § *1.56* which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Filing Date	Status - Patented, Pending or Abandoned

☐ Additional US/PCT Priority Application(s) Listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willfull false statements and the like so made are punishable by fine or imprisonment, or both, under *section 1001 of title 18 of the United States Code* and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: J. Ernest Kenney, Reg. Mo. 19,179; Eugene Mar, Reg. No.25,893; Richard E. Fichter, Reg. No. 26,382; Charles R. Wolfe, Jr., Reg. No. 28,680; Thomas J. Moore, Reg. No. 28,974; Bruce H. Troxell, Reg. No. 26,592; and

I(we) authorize my(our) attorneys to accept and follow instructions from JOU AND LIN International Patent Office regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I(we) or my(our) assigns withdraw this authorization in writing.

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DATE	SIGNATURE
1999. 6. 4	Huang, Chen-Chih

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